

Overview

The JTRS SDR Kit is intended for developing, testing and demonstrating the operation of products based on Xilinx' Virtex™-4 FPGA and the Software Communications Architecture (SCA). This SCA-enabled platform uses System-on-Chip (SoC) and Partial Reconfiguration (PR) technologies to lower substantially power consumption and component count of a Software Defined Radio (SDR) modem.

Benefits

Targeted at companies and Research laboratories designing and experimenting wireless communication systems for civilian or military applications. In military applications, it offers an ideal development environment for Joint Tactical Radio System (JTRS) providers of SCA compliant waveforms. The JTRS SDR kit allows System Engineers as well as Software, Firmware and Hardware Engineers to:

- Develop and experiment Ethernet-based SCA waveforms (ex: VoIP and streaming video)
- Develop and experiment SCA waveforms
- Develop and experiment with the SCA running on a FPGA SoC platform
- Develop and experiment FPGA-software co-design in a SCA environment
- Develop and experiment FPGA Partial Reconfiguration technology in a SCA environment
- Develop and experiment with proprietary waveforms by uploading your own proprietary design as partial bitstreams into a single FPGA
- Come up to speed quickly with on-site installation and training

JTRS SDR Kit

The JTRS SDR kit includes the following components:

- 2 IDP100 development platforms
- 2 laptops
- 2 IP Phones
- 2 Webcams
- 2 Pre-installed SCA waveforms (256 Kb/s FSK and 1024 Kb/s FSK)
- FPGA waveforms model from Xilinx System Generator
- Green-Hills Integrity 5.0.5 Board Support Package
- SCA board support package for Integrity 5
- SCA components reference design
- **PlanAhead** and access to PR lounge from Xilinx.

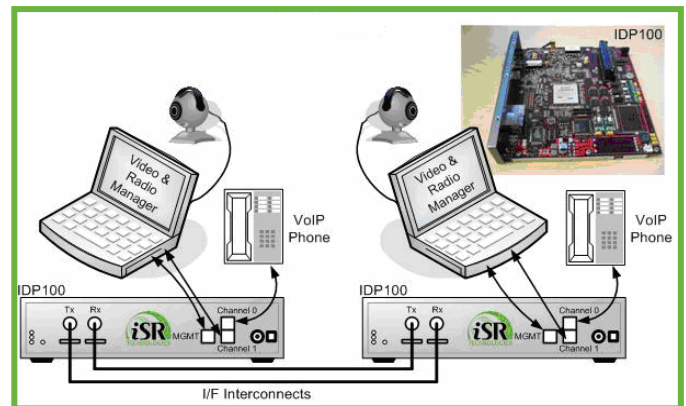


Figure 1: View of JTRS SDR Kit

Basic Configuration

The basic configuration of the kit enables the user to demonstrate and develop partial reconfigurable waveforms.

- In a PR demonstration mode, the operation of the kit enables the user to test the PR function with the two pre-installed SCA waveforms. The communication between the two IP phones is associated with the 256 Kb/s FSK waveform and the functionality of the two webcams is associated with the 1024 Kb/s waveform.
- In a PR development mode, it enables the user to select the desired proprietary waveforms, then to develop and generate the corresponding bitstream to be uploaded on the FPGA for further testing and evaluation.

IDP100 Hardware Architecture

Each Virtex™-4 based IDP100 platform provides a hardware on which partial reconfiguration waveforms may be loaded and tested in a SCA environment. The IDP100 hardware architecture has the following components:

- Xilinx' Virtex™-4 XC4VFX60-10FF1152C FPGA with embedded IBM Power PC 405 Processor
- Xilinx' SystemACE
- 128 MB DDR SDRAM
- 256 MB CompactFlash Card
- One 10/100/1000 Mb/s Ethernet Management Port
- Two 10/100 Mb/s Ethernet Data Port
- 14-bit, 300 MHz D/A Converter
- 12-bit, 180 MHz A/D Converter

Virtex™-4 FPGA contains a static infrastructure and reconfigurable components. The static infrastructure is the portion of the design which is common to all waveforms. It consists of digital up/down converters, Tx/Rx NCO, filters, and other logic relevant to the design. It is instantiated once at power up and stays valid for the duration of the uptime of the system. The reconfigurable components are the other portions of the design which can be instantiated when needed. Figure 2 shows the IDP100 hardware components block diagram indicating the static infrastructure and reconfiguration components implemented in the Virtex™-4 FPGA design.

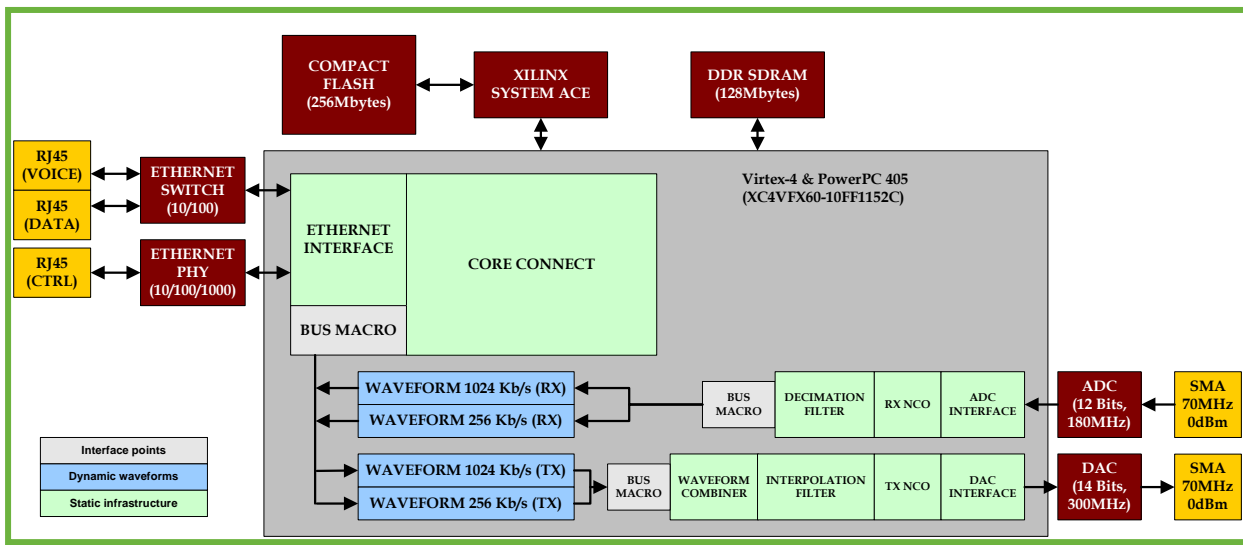


Figure 2: Block Diagram of IDP 100 hardware components

The JTRS SDR kit includes SCA components design example for running the pre-installed demonstration waveforms. Two SCA waveforms are included: a 256Kb/s FSK and a 1024Kb/s FSK waveforms. These two waveforms are supported by a complete SCA environment composed of third-party software components. The following lists the firmware and software components integrated in the kit:

Static Infrastructure	Reconfigurable Components
<p>Firmware Components</p> <ul style="list-style-type: none"> • Core Connect PPC405 - PPC405 Processor - PLB & OPB Bus - Serial Uart-Lite - PLB Ethernet Core - OPB Interrupt Controller - OPB HW ICAPS • Data Ethernet Device • Frequency Up/Down Converter 	<p>Firmware Components</p> <ul style="list-style-type: none"> • FM 256 Kb/s Modulator/Demodulator • FM 1024 Kb/s Modulator/Demodulator <p>Software Components (Executable binary)</p> <ul style="list-style-type: none"> • FM 256 Kb/s Waveform Resource • FM 1024 Kb/s Waveform Resource
<p>Software Components</p> <ul style="list-style-type: none"> • Operating Environment (runtime version) <ul style="list-style-type: none"> - Green-Hills Integrity 5.0.5 RTOS Kernel - OIS ORBExpress RT 2.6.3 CORBA - CRC SCARI++ 1.3.3 Core Framework - Interpeak's TCP/IP stack - Integrity MSDOS files system • SCA Components <ul style="list-style-type: none"> - Domain Manager (Executable binary) - Device Manager (Executable binary) - Log Service (Executable binary) - Up & Down-Converter + Ethernet Device - BSP (Source code) - PPC405 Executable Device (Source code) - Demo waveforms resources (Source code) 	

IDP100 Platform Architecture

The IDP100 platform architecture is broken down in five layers as shown in figure 3. The IDP100 comes with pre-integrated software and firmware components in addition to some source code examples that can be used as a reference by engineers to build their own waveforms.

- The first layer is the IDP100 hardware reference platform.
- The second layer is the Virtex™-4 FPGA with the static and dynamic firmware resources.
- The third layer is composed of the Real Time Operating System (RTOS), the CORBA Object Request Broker (ORB) and the SCA Core Framework.
- The fourth layer contains the SCA node devices drivers and logical devices to control the IDP100 hardware platform.
- The fifth and last layer contains the two reference SCA waveform applications.

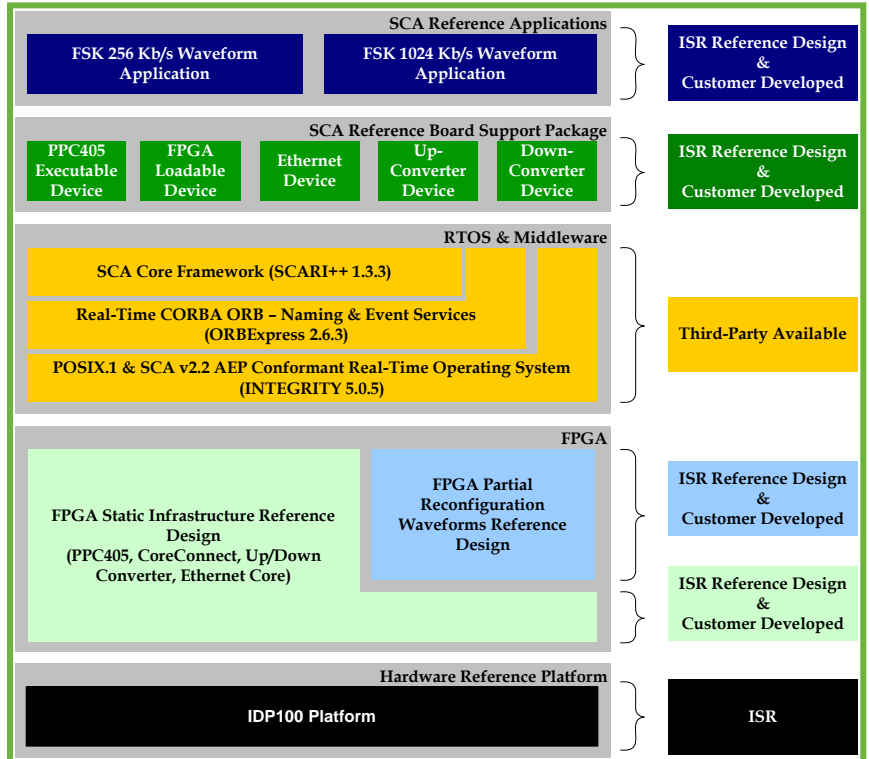


Figure 3: IDP 100 Platform Layered Architecture

Partial Reconfiguration Architecture

The Virtex™-4 FPGA has two reconfiguration regions for the firmware of the two pre-installed waveform. These reconfiguration regions have been designed with Xilinx' PlanAhead design tools and are shown in figure 6. The upper region (region A), highlighted in white on figure 6, is used for the 1024 Kb/s waveform. The available and required resources for this waveform are shown in figure 4. The lower region (region B), also highlighted in white on figure 6, is used for the 256 Kb/s waveform. The available and required resources for this second waveform are shown in figure 5. These regions can be reconfigured using partial bitstream without interrupting the operation of all other functions of the FPGA and the complete IDP100 unit.

Type of Site	Available	Required	% Utilization
DSP48	24	5	20.83
FIFO16	36	6	16.67
RAMB16	36	1	2.78
SLICEL	1,824	806	44.19
SLICEM	1,824	806	44.19
LUT	7,296	2,470	33.85
FF	7,296	2,414	33.09

Figure 4: PR Region A

Type of Site	Available	Required	% Utilization
DSP48	24	5	20.83
FIFO16	36	6	16.67
RAMB16	36	1	2.78
SLICEL	1,440	786	54.58
SLICEM	1,440	786	54.58
LUT	5,760	2,384	41.39
FF	5,760	2,388	41.46

Figure 5: PR Region B

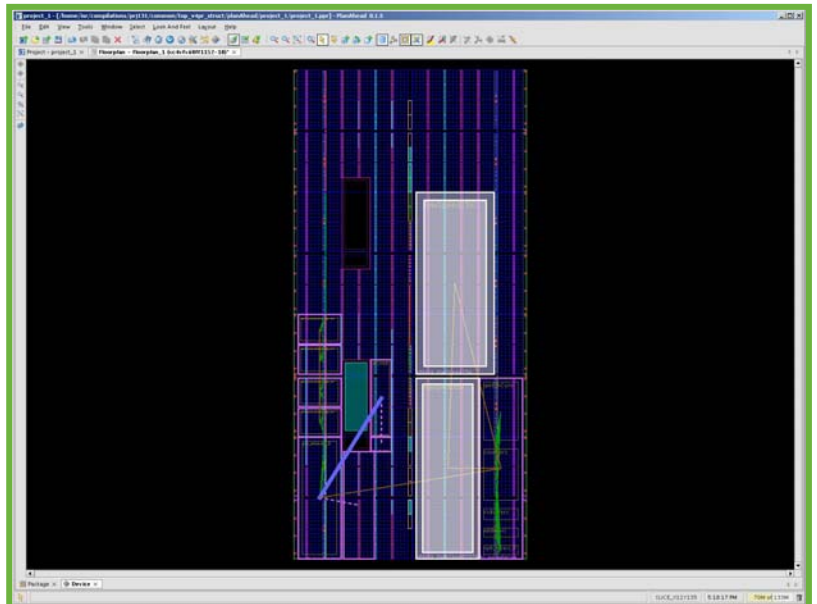


Figure 6: View of PR regions A & B on the Virtex™-4 FPGA

Third-Party Software Licenses and Tools

Beside the basic components listed above and included in the IDP 100 development kit, the following software licenses and tools are required for the development of SCA waveforms:

- Green-Hills Integrity 5.0.5 real-time operating system (www.ghs.com)
- Interpeak's IPLite TCP/IP stack
- Integrity MSDOS file system on IDP100 CompactFlash card
- Integrity BSP source code package
- ORBexpress RT 2.6.3 CORBA object request broker (www.ois.com)
- CRC's SCARI++ 1.3.3 SCA core framework (<http://www.crc.ca/en/html/crc/home/research/satcom/rars/sdr/sdr>)

ISR Technologies

ISR Technologies is a leading edge Software Defined Radio (SDR) company. By combining ISR's extensive signal processing expertise with its state of the art Software Defined Radio capabilities, ISR produces Software Defined Radio and Communication Subsystems that are unparalleled in flexibility, scalability, and performance, making them among the most advanced products in the industry.



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